IN THE CLAIMS:

1. (Currently Amended) An image processing apparatus comprising:

image input/output processing means for inputting/outputting an image;

a memory which shares different types of image data by time division;

encoding/decoding processing means for encoding or decoding data stored in the memory; and

data transfer control means for controlling a data transfer from the memory to the image input/output processing means or the encoding/decoding processing means, wherein

a first transfer data group, which can be ~~subjected to~~ scheduled for direct memory access, ~~scheduling~~ is divided into burst transfer units,

the direct memory access ~~in~~ of the burst transfer units is periodically performed, and

~~the~~ a second transfer data group, which cannot be ~~subjected to~~ scheduled for direct memory access ~~scheduling~~ is subjected to the direct memory access during at least a portion of the period that the first transfer data group is not subjected to the direct memory access; wherein

an in-progress direct memory access of the second transfer data group is suspended during a scheduled direct memory access of the first transfer data group.

2. (Currently Amended) The image processing apparatus of Claim 1 wherein

~~the~~ each burst transfer unit is obtained by equally dividing the first transfer group ~~combining a block unit into which the transfer data which can be previously subjected to the direct memory access scheduling is equally divided~~, and

~~the block unit~~ each burst transfer unit is periodically subjected to the direct memory access.

3. (Currently Amended) An image processing apparatus comprising:

image input/output processing means for inputting/outputting an image;

a memory which shares different types of image data by a time division method; and

data transfer control means for controlling a data transfer from the memory to the image input/output processing means or ~~the~~ encoding/decoding processing means, wherein

the data transfer control means comprises:

the encoding/decoding processing means ~~for encoding or decoding~~ encodes or decodes data stored in the memory;

direct memory access request generating means for generating a transfer timing of data which can be previously subjected to the direct memory access scheduling;

direct memory access request adjusting means for performing adjustment so as to interrupt the direct memory access with the encoding/decoding processing means and preferentially execute the direct memory access of the image input/output processing means in the case where the direct memory access request is made from the direct memory access request generating means;

direct memory access settings holding means for holding setting information of the direct memory access;

data transfer executing means for generating an address of the memory on the basis of direct memory access setting information to transfer data by an instruction from the direct memory access request adjusting means; and

memory control means for controlling writing or read-out of the memory.

4. (Original) The image processing apparatus of Claim 3 wherein

the direct memory access request generating means comprises:

frame detecting means for detecting the head of the frame;

first line detecting means for detecting the head of the line inside the frame;

clock counting means for receiving a line head signal from the first line detecting means to reset a discrete value, and thereafter counting an operation clock;

line counting means for receiving a frame head signal from the frame detecting means to reset a discrete value, and thereafter counting a line head signal from the first line detecting means;

second line detecting means for detecting a start time of the direct memory access in burst transfer units which can be previously subjected to the direct memory access scheduling from the discrete value of the clock counting means;

line cycle counting means for resetting the discrete value by the frame head signal from the frame detection means and a signal after one cycle end and counting the line detecting signal from the second line detecting means;

efficient vertical period detecting means for detecting an efficient line period from the discrete value of the line counting means and a detecting signal of the second line detecting signal;

efficient line detecting means for detecting an efficient line from the discrete value of the line cycle counting means; and

request signal detecting means for detecting a request timing of the direct memory access from the discrete value of the clock counting means, and

generates a direct memory access request signal from a signal output of the efficient vertical period detecting means, a signal output of the efficient line detecting means, and a signal output of the request signal detecting means.

5. (Original) The image processing apparatus of Claim 3 wherein

the direct memory access settings holding means comprises:

first control information storage means for storing control information required for data transfer control performed by the data transfer control means;

second control information storage means for holding control information required for the data transfer control concerning the direct memory access to be preferentially executed;

third control information storage means for, when the data transfer by the data transfer executing means is interrupted, saving the control information required for retransferring the data later to store; and

control information transfer means for performing a transfer of the control information among the first through third control information storage means, and a transfer of the control information between the data transfer executing means, and the second control information storage means and the third control information storage means.

6. (Original) The image processing apparatus of Claim 3 wherein

the direct memory access adjusting unit comprises:

data transfer request adjusting means for receiving a data transfer request from the encoding/decoding means or the direct memory access request generating means and selecting a classification of the data transfer to be executed next and a priority of the data transfer;

second data transfer classification holding means for holding a classification of the data transfer corresponding to the control information held by the second control information storage means;

second data transfer priority holding means for holding priority information corresponding to the control information held by the second control information storage means;

first data transfer classification holding means for holding a classification of the data transfer under the execution in the data transfer execution means;

first data transfer priority holding means for holding priority information of the data transfer which is being executed in the data transfer executing means;

third data transfer classification holding means for holding a classification of the data transfer corresponding to the control information held by the third control information storage means;

third data transfer priority holding means for holding priority information of the data transfer corresponding to the control information held by the third control information storage means; and

control information save means for executing data transfer control by using information of a reservation end flag which shows completing an obtainment of the control information by either of the data transfer request adjusting means, the first through third data transfer classification holding means, the first through third data transfer priority holding means, and the second control information holding means, and information of a save end flag which shows

completing the storage of the control information held by the third control information storage means in the first control information storage means.

7. (Original) The image processing apparatus of Claim 6 wherein

the data transfer request adjusting means selects a data transfer request which has the highest data transfer priority as well as is received earliest among the ones from which classifications of the data transfer held by the first through third data transfer classification holding means are excluded of the received data transfer requests, as the data transfer to be executed next.

8. (Original) The image processing apparatus of Claim 7 wherein

the data transfer request adjusting means comprises:

priority information registering means for registering priority information of the received data transfer request;

new data transfer request detecting means for detecting classifications of the data transfer request newly registered in the priority information registering means;

data transfer request order registering means for registering classifications of the data transfer request detected by the new data transfer request detecting means in order; and

top priority proposed data transfer detecting means for detecting a classification of the data transfer request which has the highest data transfer priority as well as is received earliest among the ones from which classifications of the data transfer held by the first through third data transfer classification holding means are excluded, from information registered by the priority

information registering means and the data transfer request order registering means, and information held by the first through third data transfer classification holding means.

9. (Original) The image processing apparatus of Claim 8 wherein

the data transfer request adjusting means changes priority information registered by the priority information registration means in accordance with the result detected by the top priority proposed data transfer detecting means.

10. (New) The image processing apparatus of claim 1, wherein a suspended direct memory access of the second transfer data group resumes after the scheduled direct memory access of the first transfer data group.

11. (New) An image processing apparatus, comprising:

an image processor configured to input and output an image;

a memory; and

data transfer controller configured to control data transfer from said memory to said image processor or an encoder/decoder, said data transfer controller comprising:

a direct memory access request generator configured to schedule direct memory access;

a direct memory access interrupter configured to interrupt direct memory access with said encoder/decoder and to execute scheduled direct memory access of said image input processor if direct memory access is request by said direct memory access request generator;

a store configured to hold setting information of direct memory access;

a data transfer executor configured to generate an address of said memory based on at least direct memory access setting information to transfer data by an instruction from the direct memory access request adjustor; and

a memory controller configured to control writing or read-out of the memory.